WHAT IS CLAIMED IS:

1. A method for interleaving SDRAM device access requests, comprising the steps of:

establishing at least one master scoreboard register having a number of bits corresponding to a number of available request cycles and wherein a value of each bit in the at least one master scoreboard register is indicative of whether an access command has been accepted for delivery to the SDRAM;

receiving an SDRAM access request from at least one device, wherein the SDRAM access requests includes at least one requested cycle for accessing the SDRAM;

identifying the bits in the at least one master scoreboard register associated with the at least one requested cycle;

determining whether at least one of the identified bits have been previously set;

accepting the SDRAM access request if it is determined that none of the identified bits have been previously set; and

performing the following steps if it is determined that at least one of the identified bits has been previously set:

incrementing the at least one master scoreboard register by one bit; and

returning, at a subsequent clock tick, to the step of identifying the bits in the at least one scoreboard register associated with the at least one requested cycle.

2. The method of claim 1, wherein the at least one master scoreboard register is a 25 bit register.

3. The method of claim 1, wherein the step of incrementing the at least one master scoreboard register, further comprises the steps of:

removing the leftmost bit in the at least one master scoreboard register;

shifting all remaining bits in the at least one master scoreboard register to the left; and

inserting a zero bit as the rightmost bit in the at least one master scoreboard register,

wherein the removed leftmost bit is indicative of any SDRAM access command going out on a next clock cycle.

4. The method of claim 1, further comprising the step of clearing all bits in the at least one master scoreboard register upon system power up.

5. The method of claim 1, further comprising the steps of:

receiving multiple simultaneous SDRAM access requests from at least two devices; and

determining a device priority to establish an order of SDRAM access requests.

6. The method of claim 1, wherein the step of accepting the SDRAM access request, further comprises the step of registering the accepted SDRAM access cycles with the at least one master scoreboard register, thereby setting the bits in the at least one master scoreboard register which correspond to the accepted SDRAM access cycles.

7. The method of claim 6, wherein the step of registering the accepted SDRAM access cycles comprises logically OR'ing the bit locations corresponding to the accepted SDRAM access cycles into the at least one master scoreboard register.

8. The method of claim 1, wherein the at least one master scoreboard register includes a data bus master scoreboard register, a command bus master scoreboard register, and a banks master scoreboard register.

9. The method of claim 8, further comprising:

identifying the bits in each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register associated with the at least one requested cycle;

determining whether at least one of the identified bits have been previously set in each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register;

accepting the SDRAM access request if it is determined that none of the identified bits have been previously set; and

performing the following steps if it is determined that at least one of the identified bits has been previously set:

incrementing each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register by one bit; and

returning, at a subsequent clock tick, to the step of identifying the bits in each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register associated with the at least one requested cycle.

10. A computer-readable medium incorporating one or more instructions for interleaving SDRAM device access requests, the instructions comprising:

one or more instructions for establishing at least one master scoreboard register having a number of bits corresponding to a number of available request cycles and wherein a value of each bit in the at least one master scoreboard register is indicative of whether an access command has been accepted for delivery to the SDRAM;

one or more instructions for receiving an SDRAM access request from at least one device, wherein the SDRAM access requests includes at least one requested cycle for accessing the SDRAM;

one or more instructions for identifying the bits in the at least one master scoreboard register associated with the at least one requested cycle;

one or more instructions for determining whether at least one of the identified bits have been previously set;

one or more instructions for accepting the SDRAM access request if it is determined that none of the identified bits have been previously set; and

one or more instructions for performing the following steps if it is determined that at least one of the identified bits has been previously set:

incrementing the at least one master scoreboard register by one bit; and

returning, at a subsequent clock tick, to the step of identifying the bits in the at least one scoreboard register associated with the at least one requested cycle.

11. The computer-readable medium of claim 10, wherein the at least one master scoreboard register is a 25 bit register.

12. The computer-readable medium of claim 10, wherein the one or more instructions for incrementing the at least one master scoreboard register, further comprise:

one or more instructions for removing the leftmost bit in the at least one master scoreboard register;

one or more instructions for shifting all remaining bits in the at least one master scoreboard register to the left; and

one or more instructions for inserting a zero bit as the rightmost bit in the at least one master scoreboard register,

wherein the removed leftmost bit is indicative of any SDRAM access command going out on a next clock cycle.

13. The computer-readable medium of claim 10, further comprising one or more instructions for clearing all bits in the at least one master scoreboard register upon system power up.

14. The computer-readable medium of claim 10, further comprising:

one or more instructions for receiving multiple simultaneous SDRAM access requests from at least two devices; and

one or more instructions for determining a device priority to establish an order of SDRAM access requests.

15. The computer-readable medium of claim 10, wherein the one or more instructions for accepting the SDRAM access request, further comprise one or more instructions for registering the accepted SDRAM access cycles with the at least one master scoreboard

register, thereby setting the bits in the at least one master scoreboard register which correspond to the accepted SDRAM access cycles.

16. The computer-readable medium of claim 15, wherein the one or more instructions for registering the accepted SDRAM access cycles comprise one or more instructions for logically OR'ing the bit locations corresponding to the accepted SDRAM access cycles into the at least one master scoreboard register.

17. The computer-readable medium of claim 10, wherein the at least one master scoreboard register includes a data bus master scoreboard register, a command bus master scoreboard register, and a banks master scoreboard register.

18. The computer-readable medium of claim 17, further comprising:

one or more instructions for identifying the bits in each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register associated with the at least one requested cycle;

one or more instructions for determining whether at least one of the identified bits have been previously set in each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register;

one or more instructions for accepting the SDRAM access request if it is determined that none of the identified bits have been previously set; and

one or more instructions for performing the following steps if it is determined that at least one of the identified bits has been previously set:

incrementing each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register by one bit; and

returning, at a subsequent clock tick, to the step of identifying the bits in each of the data bus master scoreboard register, the command bus master scoreboard register, and the banks master scoreboard register associated with the at least one requested cycle.